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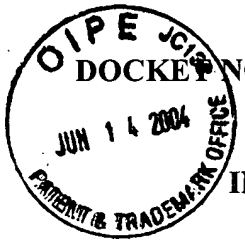

DOCKET NO. : MERCHANT 33-3-3 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Sailesh Merchant, *et al.*

Serial No.: 09/092,158

Filed: June 5, 1998

For: METHOD FOR THE FABRICATION OF CONTACTS IN AN INTEGRATED CIRCUIT DEVICE

Grp./A.U.: 2823

Examiner: Maldonado, Julio J.

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Mail Stop Appeal Brief-Patents

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June 9, 2004 Elizabeth Schumacher
Date of Mailing Signature of person mailing

ATTENTION: Board of Patent Appeals and Interferences

Sirs:

APPELLANT'S BRIEF UNDER 37 C.F.R. §1.192

This is an appeal from a Final Rejection dated February 12, 2004, of Claims 1 and 4-11, Claims 12, 15-23 and Claim 24. The Appellants submit this Brief in triplicate as required by 37

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C.F.R. §1.192(a), with the statutory fee of $ 330.00 as set forth in 37 C.F.R.§1.17(c), and hereby authorize the Commissioner to charge any additional fees connected with this communication (including extensions of time) or credit any overpayment to Deposit Account No. 08-2395.

This Brief contains these items under the following headings, and in the order set forth below in accordance with 37 C.F.R. §1.192(c):

I. REAL PARTY IN INTEREST

II. RELATED APPEALS AND INTERFERENCES

III. STATUS OF CLAIMS

IV. STATUS OF AMENDMENTS

V. SUMMARY OF INVENTION

VI. ISSUES

VII. GROUPING OF CLAIMS

VIII. PRIOR ART

IX. APPELLANTS' ARGUMENTS

X. APPENDIX A - CLAIMS

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the Assignee, Agere Systems Inc.

II. RELATED APPEALS AND INTERFERENCES

No other appeals or interferences will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 1 and 4-11, Claims 12 and 15-23, and Claim 24 are pending in this Application.

IV. STATUS OF THE AMENDMENTS

The present Application was filed on June 5, 1998. The Appellants wish to not for the record that this is the second appeal brief that the Appellants have been compelled to file in this case. The Appellants also wish to note that since the last Appeal Brief filed in November 11, 2000, the Appellants have responded to seven Office Actions issued by the Examiner, including three Final Rejections that were subsequently withdrawn. In response to the latest Final Rejection, issued in an Office Action mailed February 12, 2004, the Appellants filed a Request for Reconsideration on March 15, 2004. The Examiner issued an Advisory Action on April 2,

2004 indicating that the March 15, 2004 reply failed to put the application in condition for allowance. The Appellants filed a Notice of Appeal on April 26, 2004.

V. SUMMARY OF THE INVENTION

The present invention is directed, in general, to a method of fabricating contact plugs, and more specifically, to a method of fabricating tungsten plugs in an integrated circuit device. The present invention provides a method of forming a tungsten plug that exhibits improved contact resistance characteristics in the window provided by a thermal anneal without inducing failure of the titanium nitride layer. In general, and as presently amended, the present invention is directed to a method for fabricating a contact in a semiconductor substrate. In a claimed embodiment, the method includes depositing, by physical vapor deposition, a barrier layer in a contact opening 410 and on at least a portion of the semiconductor substrate 400. Depositing the barrier layer includes depositing a titanium layer 414 and depositing a titanium nitride layer 415 on the titanium layer 414 such as shown in FIGURE 4 (illustration 1 presents FIGUREs 4 and 5). The method also includes depositing a contact metal 435 on the barrier layer 414, 415 within the contact opening 410, also shown in FIGURE 4. A substantial portion of the contact metal 435 and the barrier layer 414, 145 is removed from the semiconductor substrate to form a contact plug 430 within the contact opening 410, with the plug 430 extending to an uppermost surface 530 of the substrate, such as shown in FIGURE 5. The contact plug 430 is then subject to a temperature from about 600°C to about 750°C to anneal the barrier layer. It is important to note that the contact plug 430 is subject to this temperature range after the removal process. This

avoids the damaging effects of thermal anneals done immediately after the deposition of the titanium layer 414 and titanium nitride layer 415.

FIG. 4

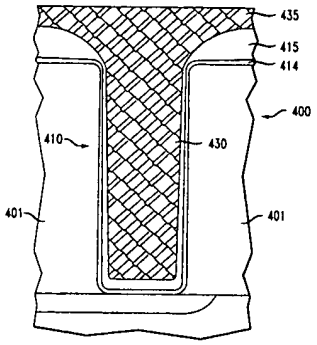


FIG. 5

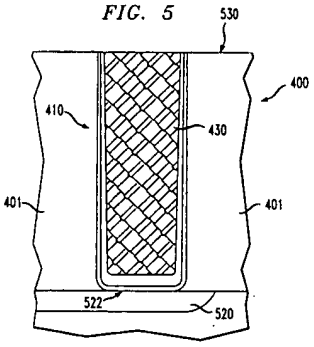


Illustration 1

Thus in one embodiment, the present invention provides a method wherein the thermal anneal is performed after removal of unwanted portions of the metal 435, titanium 414 and titanium nitride 415 layers, thereby minimizing exposure of the titanium nitride layer 415 to an annular cross section. It is also noteworthy that the TiN layer 415 in the plug 430 is very thin, approximately 5%-20% of the original field film thickness. Since only a fraction of the former field thickness is present during the thermal anneal, the advantages of producing $TiSi_x$ at the contact surface 522 (FIGURE 5) during the thermal anneal are achieved, while avoiding the damaging effects associated with conventional processes that perform thermal anneals earlier in the tungsten plug formation process.

VI. ISSUES

A. First Issue Presented for Consideration in this Appeal:

Whether Claims 1, 5-11, 12 and 16-23 and 24 as rejected by the Examiner, are patentably nonobvious in accordance with 35 U.S.C. §103(a) over U.S. Patent No. 5,591,671 to Kim *et al.* ("Kim") in view of U.S. Patent No. 5,714,418 to Bai *et al.* ("Bai") and U.S. Patent No. 5,970,374 to Teo ("Teo").

B. Second Issue Presented for Consideration in this Appeal:

Whether Claims 4 and 15, as rejected by the Examiner, is patentably nonobvious in accordance with 35 U.S.C. §103(a) over Kim in view of Bai and further in view of the Appellant's admitted prior art ("AAPA").

VII. GROUPING OF THE CLAIMS

Claims 1 and 4-11; Claims 12 and 15-23; and Claim 24 do not stand or fall together. Independent Claims 1, 12 and 24 form a first group. The dependent Claims form the following groups: Claims 4 and 15 form a second group, Claims 5-6 and 16-17 form a third group, Claims 7 and 18 form a fourth group, and Claims 8-9 and 19-20 form a fifth group, Claims 10-11 and 21-22 form a sixth group and Claim 23 forms a seventh group .

VIII. SUMMARY OF REFERENCES RELIED ON BY THE EXAMINER

A. Kim

Kim is directed to a method for interconnecting layers in a semiconductor device, which can form a low resistance contact (Abstract). A titanium ohmic contacting layer and a titanium nitride barrier layer are formed in the interior of an opening hole and on an insulating layer in sequence (Abstract). Thereafter, a refractory metal layer which completely fills the remainder of the opening hole by depositing the refractory metal on the barrier layer is formed (Abstract). To improve a contacting property, the resultant structure is heat-treated at a temperature above 450°C (Abstract). Kim states that it is desirable that the heat treatment be performed at a high temperature of about 500°C (Column 2, Line 9-11). Kim, however, is also concerned with preventing oxidation of his ohmic contact and barrier layers when heated at a temperature of about 500°C because this deteriorates their contact resistance due to oxide formation (Column 2, Lines 8-22). Kim states that this phenomenon is severe when the heat treatment temperature is above 500°C (Column 2, Lines 18-19). To reduce oxidation, Kim deposits the refractory metal layer 28 on the whole surface of the structure shown in FIGURE 2D, and then heats the resultant structure shown in FIGURE 2E (both FIGUREs 2D and 2E are presented in illustration 2) at a temperature above 450°C, and more preferably at 500°-550°C (Column 4, Lines 62-64). Among the several examples given by Kim, heating beyond 550°C is never disclosed or suggested (*see e.g.*, Column 6, Lines 18-24).

FIG. 2D

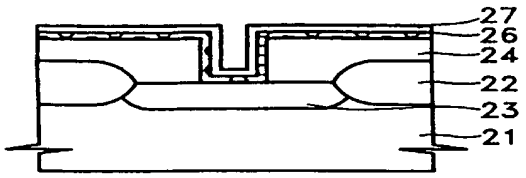


FIG. 2E

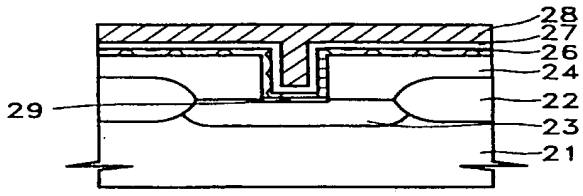


Illustration 2

In one embodiment, the refractory metal 28, ohmic contact layer 26 and barrier layer 27 on insulating layer 24 is etched-back, thereby leaving the metal only in the contact hole (Column 5, Lines 61-66), as shown in FIGURE 4B (illustration 3). The metal 28 is etched back below the level of the substrate to accommodate the deposit of an oxidation preventing cap layer 34 (Column 5 Line 66-67), shown in FIGURE 4C (illustration 3). Thereafter, the resultant structure is heated (Column 6 Line 1-3).

FIG. 4B

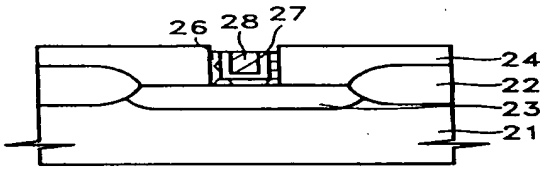


FIG. 4C

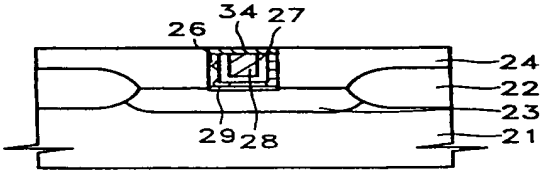


Illustration 3

B. Bai

Bai is directed to an electrical interconnect structure with a bi-layer diffusion barrier, comprising a capturing layer beneath a blocking layer, and a method of forming the structure over a semiconductor substrate (Abstract). After forming capture layer 43 and blocking layer 42, as shown in FIGURE 4B (illustration 4 presents FIGUREs 4B-4D), but before depositing the conductive layer of copper, Bai subjects the bi-layer diffusion barrier to an optional high temperature process step to anneal the barrier at 500°C (Column 8, Lines 58-64). Bai does this to anneal micro defects in the barrier layer so that the barrier layer can be more effective in preventing diffusion of Copper atoms into the device (Column 3, Lines 56-66; Column 8, Lines 63-65). Subsequently, as shown in FIGURE 4C, Bai deposits a copper layer 44 (Column 9, Lines 4-11). Later, Bai performs a chemical mechanical polishing (CMP) process to remove the copper layer 44, blocking layer 42 and capturing layer 43 from the upper surface of the dielectric layer (41) (Column 9, Line 12-19; FIGURE 4D). But there is no suggestion of performing a thermal anneal after the CMP process.

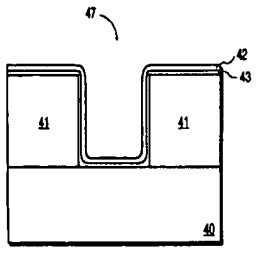


FIG. 4B

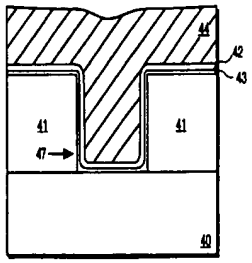


FIG. 4C

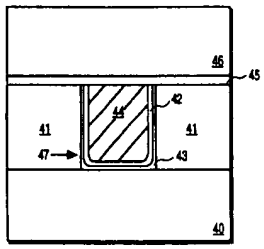


FIG. 4D

Illustration 4

C. Teo

Teo is directed to a method for forming void-free, low resistance tungsten plug contacts and vias within openings having a Ti-TiN metallurgy deposited by PVD techniques, such as sputtering (Column 3, Lines 15-19). Teo deposits a Ti layer 16 and a TiW layer 18 (Column 4, Lines 17-22) into an opening as shown in FIGURE 3A (see illustration 5, presenting FIGUREs 3A-3F) and then subjects this structure to a rapid thermal anneal of 670°C for 30 seconds (Column 4, Lines 17-22). Teo then partially fills the contact opening with spin-on-glass, SOG 26 (Column 4, Lines 33-48; FIGURE 3B), then performs CMP until the final design thickness 24 is reached (Column 4, Lines 49-58)FIGURE 3C), and then removes the SOG 26 (Column 4, Lines 59-63; FIGURE 3D). After depositing a barrier layer 30, tungsten 40 is deposited in the opening and then etched back to define the tungsten plug 42 (FIGUREs 3E-3F; Column 4 Line 64 to Column 5 Line 15).

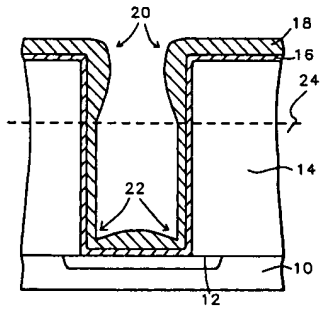


FIG. 3A

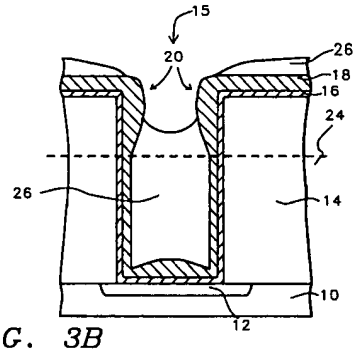


FIG. 3B

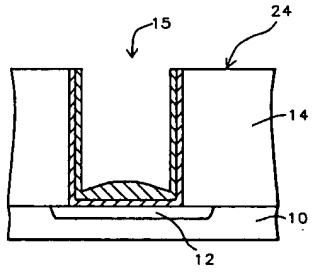


FIG. 3C

Illustration 5

I

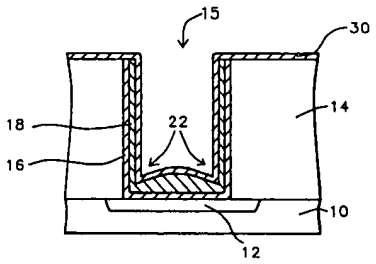


FIG. 3D

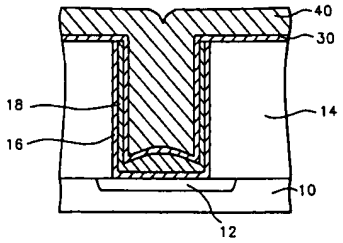


FIG. 3E

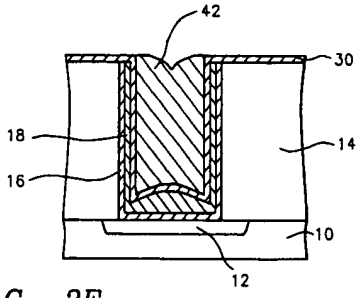


FIG. 3F

llustration 5 (continued)

D. Appellant's Admitted Prior Art

The Appellant's Prior Art acknowledges that aspect ratios of contacts, *i.e.*, the ratio of the opening depth to the opening diameter, have increased from an order of about 1:1 or 2:1 to a present order of from about 3:1 to as high as about 5:1 for sub-0.25 micron devices (Page 2, Lines 2-6).

IX. THE APPELLANTS' ARGUMENTS

The inventions set forth in independent Claims 1, 12, and 24 and their respective dependent claims are not obvious in view of the references on which the Examiner relies because the references of Kim in view of Bai and Teo fails to teach or suggest all elements of the claimed inventions and because the references of Kim and Bai, and Kim in view of Bai and Teo, are not properly combined.

A. Rejection of Claims 1, 12 and 24 under 35 U.S.C. §103 (a)

The Examiner acknowledges that Kim fails to show extending a plug to an uppermost surface of the substrate (Page 5 of Examiner's Office Action mailed February 12, 2004). The Examiner cites

Bai, referring to FIGUREs 4C-4D, for the proposition of teaching the steps of removing a substantial portion of a contact metal (44) and barrier layer (42,43) from a semiconductor substrate (40,41) to form a contact plug within a contact opening (47), the plug extending to an uppermost surface of the substrate (40,41). The Examiner believes one of ordinary skill in the art would be motivated to enable the removing step of Kim to be performed according to Bai because this would isolate the interconnect layer within the trench. Citing MPEP 2144.07, the Examiner further states that one would look to alternative suitable methods of performing the removing step of Kim that are recognized as suitable for an intended purpose. The Appellant respectfully disagrees.

It is well established that to establish a *prima facie* case of obviousness, three criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure. See MPEP §2143 - §2143.03 for decisions pertinent to each of these criteria.

As is well settled, "[o]bviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys., Inc. v. Montefiore Hosp.*, 732 F.2d 1572,1577, 221 USPQ 929, 933 (Fed. Cir. 1984). The case law also makes clear that one "cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *Ecolochem, Inc. v. So. California Edison*, 56 USPQ2d 1065, 1073 (Fed. Cir. 2000), *In re Fine*, 837

F.2d 1071,1075, 5 USPQ2d 1780, 1783 (Fed. Cir. 1988). Hindsight knowledge of the Applicants' disclosure when the prior art does not teach or suggest such knowledge, results in the use of the invention as a template for its own reconstruction. This is inappropriate in the determination of patentability. *Sensonics Inc. v. Garlock, Inc.*, 220 USPQ 303, 312-313 (1983). Moreover, where the inventor has achieved the claimed invention by doing what those skilled in the art suggested should not be done is a fact strongly probative of nonobviousness. *Kloster Speedsteel AB v. Crucible Inc.*, 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 19860, on rehearing, 231 USPQ 160 (Fed. Cir. 1986).

Because of the disparate teachings of Kim and Bai, one skilled in the art would not be motivated to combine their teachings. First, the Appellants wish to note that the section of the MPEP 2144.07 cited by the Examiner presents case law which discusses the *selection of known materials* based on their suitability to support a *prima facie* obviousness determination, and not the *selection of known methods*. The Appellants submit that extending MPEP 2144.07 to methods goes beyond the supporting case law.

Second, the Appellants submit that one skilled in the art would not be motivated to incorporate Bai's removing method into Kim's removing step in the manner suggested by the Examiner, because there is no suggestion or motivation in the references themselves to support their combination, and there is not a reasonable expectation of success. Introducing new, or switching steps, in a process, such as a process flow for semiconductor fabrication, can have unpredictable consequences and therefore a change in a process flow is not done without a strong motive to do so.

As noted above, Kim performs a heat treatment either after depositing the refractory metal layer 28 on the whole surface of the structure shown in FIGURE 2D, or after etching back the metal 28 to be only in the opening and then forming a protective oxidation cap 34 over the metal plug 28

in the opening, as shown in FIGURE 4C. Kim does this to avoid the deleterious effects of oxidation of the ohmic contact and barrier layers during Kim's heat treament. It is clear, therefore, that Kim does not wish to use a removing step that would result in either the ohmic contact and barrier layers being oxidized during the heat treatment

The Examiner proposes using Bai's CMP method of removing a substantial portion of a contact metal and barrier layer from a semiconductor substrate, instead of Kim's method of etching back followed forming a protective oxidation cap 34. Bai's method of removing is not suitable for use in Kim process flow, because it would expose portions of Kim's barrier layer to oxidation during thermal annealing, which Kim expressly wishes to avoid. Therefore, contrary to the Examiner's proposal, Bai's method is not a suitable alternative method for Kim's purpose. The Appellant respectfully submits that the Examiner has improperly used the present invention as a template for his own reconstruction, and then used hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.

The Examiner also acknowledges that the combined teachings of Kim and Bai do not teach a temperature range from about 600°C to about 750°C to anneal the barrier layer (Page 5 of Examiner's Office Action mailed February 12, 2004). To remedy the deficient teachings of Kim and Bai, the Examiner cites Teo. The Examiner states that it would be obvious to one of ordinary skill in the art to use the rapid thermal anneal process taught by Teo in the combination of Kim in view of Bai because this improves the adhesion of the barrier layer in the contact layer.

The Appellants respectfully submit that Teo does not teach or suggest the elements of subjecting a contact plug to a temperature from about 600°C to about 750°C to anneal the barrier

layer of Claim 1. The Appellants further submit that Teo is not properly combinable with the combination of Kim in view of Bai

First, the Appellants wish to point out that Kim in view Bai do not teach subjecting a contact plug, as defined in Claim 1, to an elevated temperature. In fact, the Examiner is on the record, stating that the combination of Kim in view of Bai fails to teach subjecting the contact plug to a temperature sufficient to anneal the barrier layer (Page 3, Line 11-12, of the Examiner's Office Action mailed June 11 and Page 3, Lines 14-15, of the Examiner's Office Action mailed January 3, 2003).

Claim 1 recites that the contact plug is within the contact opening, the plug extending to an uppermost surface of the substrate. Therefore the contact plug that is subjected to a temperature from about 600°C to about 750°C is a plug that extends to the uppermost surface of the substrate. Neither Kim, Bai nor Teo disclose subjecting such a contact plug to this temperature range.

As noted above, Kim performs a thermal anneal on the structure shown in FIGURE 2E, after depositing the refractory metal layer 28 on the whole surface of the structure shown in FIGURE 2D. Alternatively Kim performs a heat treatment only after both etching back the metal 28 to be only in the opening and forming a protective oxidation cap 34 over the metal plug 28 in the opening, as shown in FIGURE 4C. Therefore, neither of the structures shown in FIGURE 2E or 4C that are heated by Kim have a contact plug as defined in Claim1. This follows because neither of Kim's structures extend to an uppermost surface of the substrate. In the structure shown in FIGURE 2E, the refractory metal layer 28 extends beyond uppermost surface of the substrate, while in the structure shown in FIGURE 4C, the metal 28 is below the uppermost surface of the substrate.

In contrast to Kim, Bai performs a high temperature process step after forming the bi-layer

diffusion barrier of the capture layer 43 and blocking layer 42, shown in FIGURE 4B, but before depositing the conductive layer of copper. As noted above, Bai does this to cure micro defects so that the barrier layer can be more effective at preventing diffusion of Copper atoms into the device. Therefore, Bai also does not teach subjecting a contact plug to an elevated temperature.

Therefore, the Examiner must rely on Teo, not only to teach a temperature range from about 600°C to about 750°C, but also to teach subjecting a contact plug to such a temperature range.

Teo, however, does not subject his contact plug to an elevated temperature. Teo clearly indicates (Column 4, Lines 17-22) that it is the structure shown in FIGURE 3A that can be subjected to an optional rapid thermal anneal of 670°C for 30 seconds. The structure shown in FIGURE 3A, however, does not have a contact plug. In fact, the opening is not filled with tungsten until Teo's process flow has progressed to the stage shown in FIGURE 3D. Moreover, Teo provides no teaching or suggestion of performing a thermal anneal after depositing a contact metal on a barrier layer within the contact opening and after removing a substantial portion of the contact metal and the barrier layer from the semiconductor substrate to form a contact plug.

Second, the Appellants submit that Teo is not properly combinable with Kim in view of Bai because one of ordinary skill in the art would not be motivated to use Teo's annealing temperature range in Kim's heat treament. Kim is concerned with preventing oxidation of his ohmic contact (*e.g.* Ti) and barrier (*e.g.*, TiN) layers when heated at a temperature of about 500°C, because this severely deteriorates their contact resistance (Column 2, Lines 8-22). To reduce oxidation, Kim deposits the refractory metal layer 28 on the whole surface of the structure shown in FIGURE 2D and then heats the resultant structure shown in FIGURE 2E at a temperature above 450°C, and more preferably, at 500°-550°C. As noted above, Kim does not disclose or suggest heating beyond 550°C.

In contrast, Teo performs an optional rapid thermal anneal (RTA) at 670°C *after* the deposition of a Ti layer 16 and a TiW layer 18 (Column 4, Lines 17-25; FIG. 3A), but *before* the deposition of tungsten 40 (Column 5, Lines 3-8; FIGURE 3E). Thus Teo's RTA is conducted at a much earlier point in the fabrication process than the heating step used in Kim's process.

The Applicants maintain that there is no motive for one skilled in the art to apply Teo's RTA of 670°C to the heat treatment in Kim's process. The Examiner seeks to use Teo's statement that RTA activates the carriers in the silicon and forms strong chemical bonds to the Ti as the motive for inserting Teo's RTA into Kim's process. Kim, however, is trying to balance the benefits of heating above 450°C to improve the interconnection properties of the ohmic contact and barrier layers (Column 1, Lines 60-62), against severe oxidation of these layers at temperatures above 500°C (Column 2, Lines 13-22). Even with his refractory metal layer 28 in place, however, Kim is careful not to heat beyond 550°C. There is no reason why one skilled in the art would be motivated to heat Kim's ohmic contact and barrier layers beyond Kim's limit of 550°C, based on Teo's teaching of performing a RTA of Ti and TiW layers in an unfilled contact opening 15 shown in Teo's FIGURE 3A. Moreover, because Teo's RTA is conducted at a different point in the fabrication process than Kim's heating step, one skilled in the art would be extremely reluctant to change Kim's heating step to Teo's RTA.

Given that Kim uses temperatures up to 550°C, one skilled in the art would not have sufficient motive to change the heating step to 600°C and beyond. The Applicants respectfully submit that the Examiner is improperly using hindsight reconstruction to pick and choose among isolated disclosures from Kim and Teo to deprecate the claimed invention.

Thus, because the references of Kim in view of Bai and Teo do not teach or suggest all elements of the present invention and are not properly combinable, the Examiner has failed to establish a *prima facie* case of obviousness with respect to independent Claim 1. A similar conclusion applies to independent Claim 12 and 24 which contains elements analogous to that discussed for Claim 1 above. Accordingly, the Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claims 1, 12 and 24.

B. Rejection of Claim 4 and 15 under 35 U.S.C. §103 (a)

The Examiner has rejected these claims based on the combined teachings of the Kim in view of Bai as applied to Claims 1 and 5-11 and Claims 12 and 16-23, and further in view of the AAPA. Dependent Claims 4 and 15 require forming a contact opening having an aspect ratio ranging from about 3:1 to about 5:1, and thereby introduce patentably distinct elements as applied in combination with the elements recited in Claims 1 and 12, respectively.

The Appellants submit that the combination of Kim in view of Bai and the AAPA fails to establish a *prima facia* case of obviousness with respect to Claims 4 and 15 because these references do not teach or suggest all the elements of these claims and because, and as argued above and incorporated herein by reference, Kim in view of Bai are not properly combinable.

Claims 4 and 15 depend on Claims 1 and 12, and therefore includes each and every element of Claim 1 and 12, respectively, including the element of subjecting the contact plug to a temperature from about 600°C to about 750°C to anneal the barrier layer. By the Examiner's own admission (Page 5 of Examiner's Office Action mailed February 12, 2004), the combined teachings of Kim and Bai do not teach a temperature range from about 600°C to about 750°C to anneal the barrier layer.

The APAA is cited by the Examiner solely for the proposition of teaching an opening having an aspect ratio ranging from about 3:1 to about 5:1. Therefore the combination of Kim in view of Bai and the AAPA fails to teach or suggest all elements of the invention of Claim 4. In addition, the above arguments, establishing the nonobviousness of independent Claims 1 and 12 with respect to Kim in view of Bai and Teo, are incorporated herein by reference. Accordingly, Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claims 4 and 15.

C. Rejection of Claims 5-6 and 16-17 under 35 U.S.C. §103(a)

The Examiner has rejected Claims 5-6 and 16-17 under 35 U.S.C. §103(a) as being unpatentable over Kim in view of Bai and Teo. The above arguments, establishing the nonobviousness of independent Claims 1 and 12 with respect to these references, are incorporated herein by reference. Dependent Claims 5-6 and 16-17 additionally require that depositing a contact metal includes depositing tungsten and depositing the tungsten by chemical vapor deposition and thereby introduce patentably distinct elements in addition to the elements recited in their respective base independent claims. Kim in view of Bai and Teo, however, does not teach or suggest these elements in combination with the elements of the respective base claims. Moreover, as discussed above, the combination of Kim in view of Bai and Teo is not a proper combination of references. Thus, Kim in view of Bai and Teo does not establish a *prima facie* case of obviousness of dependent Claims 5-6 and 16-17. Accordingly, Claims 5-6 and 16-17 are nonobvious over Kim in view of Bai and Teo and the Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claims 5-6 and 16-17.

D. Rejection of Claims 7 and 18 under 35 U.S.C. §103(a)

The Examiner has rejected Claims 7 and 18 under 35 U.S.C. §103(a) as being unpatentable over Kim in view of Bai and Teo. The above arguments, establishing the nonobviousness of independent Claims 1 and 12 with respect to these references, are incorporated herein by reference. Dependent Claims 7 and 18 additionally require subjecting the contact plug to a rapid thermal anneal process and the applying rapid thermal anneal process for a period ranging from about 5 seconds to about 60 seconds, and thereby introduce patentably distinct elements in addition to the elements recited in their respective base independent claims. Kim in view of Bai and Teo, however, does not teach or suggest these elements in combination with the elements of the respective base claims. Moreover, as discussed above, the combination of Kim in view of Bai and Teo is not a proper combination of references. Thus, Kim in view of Bai and Teo does not establish a *prima facie* case of obviousness of dependent Claims 7 and 18. Accordingly, Claims 7 and 18 are nonobvious over Kim in view of Bai and Teo and the Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claims 7 and 18.

E. Rejection of Claims 8-9 and 19-20 under 35 U.S.C. §103(a)

The Examiner has rejected Claims 8-9 and 19-20 under 35 U.S.C. §103(a) as being unpatentable over Kim in view of Bai and Teo. The above arguments, establishing the nonobviousness of independent Claims 1 and 12 with respect to these references, are incorporated herein by reference. Dependent Claims 8-9 and 19-20 additionally require that depositing a barrier layer includes forming a thickness of the barrier layer ranging from about 5 nm to about 20 nm within the contact opening, and forming a field area thickness of said barrier layer on the

semiconductor substrate of about 75 nm or greater, and wherein the thickness of the barrier layer within the contact opening is about 5% to about 20% of said field area thickness. Thus, Claims 8-9 and 19-20 introduce patentably distinct elements in addition to the elements recited in their respective base independent claims. Kim in view of Bai and Teo, however, does not teach or suggest these elements in combination with the elements of the respective base claims. Moreover, as discussed above, the combination of Kim in view of Bai and Teo is not a proper combination of references. Thus, Kim in view of Bai and Teo does not establish a *prima facie* case of obviousness of dependent Claims 8-9 and 19-20. Accordingly, Claims 8-9 and 19-20 are nonobvious over Kim in view of Bai and Teo and the Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claims 8-9 and 19-20.

F. Rejection of Claims 10-11 and 21-22 under 35 U.S.C. §103(a)

The Examiner has rejected Claims 10-11 and 21-22 under 35 U.S.C. §103(a) as being unpatentable over Kim in view of Bai and Teo. The above arguments, establishing the nonobviousness of independent Claims 1 and 12 with respect to these references, are incorporated herein by reference. Dependent Claims 10-11 and 21-22 additionally require that removing a substantial portion includes removing the contact metal and the barrier layer from the field area thickness, and that removing the contact metal and the barrier layer includes removing the contact metal and the barrier layer by chemical/mechanical polishing processes. Thus Claims 10-11 and 21-22 introduce patentably distinct elements in addition to the elements recited in their respective base independent claims. Kim in view of Bai and Teo, however, does not teach or suggest these elements in combination with the elements of the respective base claims. Moreover, as discussed above, the

combination of Kim in view of Bai and Teo is not a proper combination of references. Thus, Kim in view of Bai and Teo does not establish a *prima facie* case of obviousness of dependent Claims 10-11 and 21-22. Accordingly, Claims 10-11 and 21-22 are nonobvious over Kim in view of Bai and Teo and the Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claims 10-11 and 21-22.

G. Rejection of Claim 23 under 35 U.S.C. §103(a)

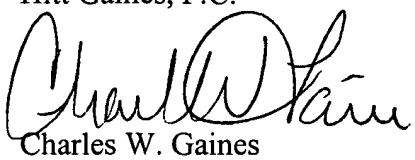
The Examiner has rejected Claim 23 under 35 U.S.C. §103(a) as being unpatentable over Kim in view of Bai and Teo. The above arguments, establishing the nonobviousness of independent Claim 12 with respect to these references, are incorporated herein by reference. Dependent Claim 23 additionally require that forming the active device includes forming an active device having a design width of about 0.25 microns or less, and thereby introduce patentably distinct elements in addition to the elements recited in its base independent claim. Kim in view of Bai and Teo, however, does not teach or suggest these elements in combination with the elements of its base claim. Moreover, as discussed above, the combination of Kim in view of Bai and Teo is not a proper combination of references. Thus, Kim in view of Bai and Teo does not establish a *prima facie* case of obviousness of dependent Claim 23. Accordingly, Claim 23 is nonobvious over Kim in view of Bai and Teo and the Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claim 23.

In conclusion, for the reasons set forth above, the Claims on appeal are patentably nonobvious over the combination of Kim in view of Bai and Teo, or the combination of Kim in view

of Bai and the AAPA (Claims 4 and 15). Accordingly, the Appellant respectfully requests that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of all of the Appellant's pending claims.

Respectfully submitted,

Hitt Gaines, P.C.



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X. APPENDIX A - CLAIMS

1. A process for fabricating a contact in a semiconductor substrate having a contact opening formed therein, comprising:

depositing by physical vapor deposition a barrier layer in said contact opening and on at least a portion of said semiconductor substrate, wherein said depositing said barrier layer includes depositing a titanium layer and depositing a titanium nitride layer on said titanium layer;

depositing a contact metal on said barrier layer within said contact opening;

removing a substantial portion of said contact metal and said barrier layer from said semiconductor substrate to form a contact plug within said contact opening, said plug extending to an uppermost surface of said substrate; and

subjecting said contact plug to a temperature from about 600°C to about 750°C to anneal said barrier layer.

4. The process of Claim 1 wherein said depositing said barrier layer includes depositing said barrier layer in said contact opening formed in a dielectric and having an aspect ratio ranging from about 3:1 to about 5:1.

5. The process of Claim 1 wherein said depositing a contact metal includes depositing tungsten.

6. The process of Claim 5 wherein said depositing includes depositing said tungsten by chemical vapor deposition.

7. The process of Claim 1 wherein said subjecting includes subjecting said contact plug to a rapid thermal anneal process.

8. The process of Claim 1 wherein said depositing a barrier layer includes forming a thickness of said barrier layer ranging from about 5 nm to about 20 nm within said contact opening and forming a field area thickness of said barrier layer on said semiconductor substrate of about 75 nm or greater.

9. The process of Claim 8 wherein said thickness of said barrier layer within said contact opening is about 5% to about 20% of said field area thickness.

10. The process of Claim 8 wherein removing a substantial portion includes removing said contact metal and said barrier layer from said field area thickness.

11. The process of Claim 10 wherein said removing said contact metal and said barrier layer includes removing said contact metal and said barrier layer by chemical/mechanical polishing processes.

12. A process for fabricating an integrated circuit, comprising:

forming an active device on a semiconductor substrate;

forming a contact opening in a dielectric deposited on said active device, said contact opening in electrical contact with said active device;

depositing by physical vapor deposition a barrier layer in said contact opening and on at least a portion of said semiconductor substrate, wherein said depositing said barrier layer includes depositing a titanium layer and depositing a titanium nitride layer on said titanium layer;

depositing a contact metal on said barrier layer within said contact opening;

removing a substantial portion of said contact metal and said barrier layer from said semiconductor substrate to form a contact plug within said contact opening, said plug extending to an uppermost surface of said substrate; and

subjecting said contact plug to a temperature from about 600°C to about 750°C to anneal said barrier layer.

15. The process of Claim 12 wherein said forming said contact opening includes forming said contact opening having an aspect ratio ranging from about 3:1 to about 5:1.

16. The process of Claim 12 wherein said depositing a contact metal includes depositing tungsten.

17. The process of Claim 16 wherein said depositing includes depositing said tungsten by chemical vapor deposition.

18. The process of Claim 12 wherein said subjecting includes subjecting said contact plug to a rapid thermal anneal process for a period ranging from about 5 seconds to about 60 seconds.

19. The process of Claim 12 wherein said depositing a barrier layer includes forming a thickness of said barrier layer ranging from about 5 nm to about 20 nm within said contact opening and forming a field area thickness of said barrier layer on said semiconductor substrate of about 75 nm or greater.

20. The process of Claim 19 wherein said thickness of said barrier layer within said contact opening is about 5% to about 20% of said field area thickness.

21. The process of Claim 19 wherein removing a substantial portion includes removing said contact metal and said barrier layer from said field area thickness.

22. The process of Claim 21 wherein said removing said contact metal and said barrier layer includes removing said contact metal and said barrier layer by chemical/mechanical polishing processes.

23. The process of Claim 12 wherein forming said active device includes forming an active device having a design width of about 0.25 microns or less.

24. A process for fabricating a contact in a semiconductor substrate having a contact opening formed therein, comprising:

depositing a barrier layer in said contact opening and on at least a portion of said semiconductor substrate, wherein said depositing said barrier layer includes depositing a titanium layer and depositing a titanium nitride layer on said titanium layer;

depositing a contact metal on said barrier layer within said contact opening;

removing a substantial portion of said contact metal and said barrier layer from said semiconductor substrate to form a contact plug within said contact opening, said plug extending to an uppermost surface of said substrate; and

subjecting said contact plug to a temperature from about 600°C to about 750°C to anneal said barrier layer.